UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/773,059	02/04/2004	Bohumil Lojek	ATM-275	5441

3897 7590 09/07/2005

SCHNECK & SCHNECK
P.O. BOX 2-E
SAN JOSE, CA 95109-0005

EXAMINER	
SOFOCLEOUS, ALEXANDER	
ART UNIT	**PAPER NUMBER**
2824	

DATE MAILED: 09/07/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/773,059	LOJEK, BOHUMIL
	Examiner	Art Unit
	Alexander Sofocleous	2824

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-35* is/are pending in the application.

4a) Of the above claim(s) *13-19 and 22-35* is/are withdrawn from consideration.

5)☒ Claim(s) *1-12,20* is/are allowed.

6)☒ Claim(s) *21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 February 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *(2) 5-19,24-2004*.
4) ☒ Interview Summary (PTO-413) Paper No(s)/Mail Date. *(2) 9/1/2005*.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: *Search History*.

DETAILED ACTION

1. This action is responsive to the following communications: the Application filed on February 4, 2004, the Information Disclosure Statement filed on May 19, 2004 and the Information Disclosure Statement filed on May 24, 2004.

2. Claims 1-35 are pending in the case. Claims 1, 13, 20, 21, 22, and 32 are independent claims.

Election/Restrictions

Restriction to one of the following inventions is required under 35 U.S.C. 121:

Group I. Claims 1-12, 20, and 21, drawn to storage device, classified in class 365, subclass 185.28.

Group II. Claims 13-19, drawn to memory structure, classified in class 257, subclass 319.

Group III. Claims 22-35, drawn to memory structure, classified in class 257, subclass 320.

The inventions are distinct, each from the other because:

Inventions Group I and Group II/III are related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct from each other if they are shown to be separately usable. In the instant case, invention Group II/III has separate utility such as not requiring simultaneous write and erase operations. See MPEP § 806.05(d).

Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification, restriction for examination purposes as indicated is proper.

During a telephone conversation with Thomas Schneck on 9/1/2005 a provisional election was made without traverse to prosecute the invention of Group I, claim1-12, 20, and 21. Affirmation of this election must be made by applicant in replying to this Office action. Claims 13-19 and 22-35 withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

Drawings

The drawings are objected to as failing to comply with 37 CFR 1.84(p)(4). The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5). Numerous inconsistencies between the specification and the figures exist. The figure(s) show reference characters that are not described in the specification. The figure(s) show multiple instances of the same number representing more than one distinct component. The same character reference is used to depict different components across the figures. The figure(s) are inconsistent with each other regarding the positioning and labeling of components. The following are examples of some of the inconsistencies. It is suggested that the applicant carefully review all of the specification and all of the accompanying figures for correctness and consistency.

The following reference character(s) are shown in the figures but are not mentioned in the description: "16" (Fig. 1), "133" (Fig. 1), "90" (Fig. 3), "91" (Fig. 3), "93" (Fig. 3), "94" (Fig. 3), and "201" (Fig. 4). Examiner assumes "133" is an actuation line similar to "33." Although "90" is described as a tang (page 7 line 15), tang "90" is not shown on Fig. 2. "90" on Fig. 3 appears to be a conductive via with unidentified component "91" attached. "93" appears to be similar to unidentified "91" and "94" appears to be similar to "90."

The reference character "28" is used to designate a cathode (Page 4 line 21 and Fig. 1), a contact (Page 9 line 8 and Fig. 1). Examiner assumes that applicant intends "28" to be the cathode of the diode labeled "29." Also, "29" is a direction arrow on tang "76" and a diode on Fig. 2. Examiner assumes that applicant intended "29" to be the diode.

Fig. 2 shows tang "76," as part of plate "100" that is capactively coupled to word line "102," connecting to transistor "21"; whereas Fig. 4 shows tang "76," as part of plate "130" that is capactively coupled to word line "119," connecting to transistor "21." Also, Fig. 3 shows characters "86" and "88" as a poly gate and source, respectively; whereas, Fig. 2 shows "86" and "88" to both be tangs on plate "30." Also, the orientation and placement of diode "29" is different on Fig. 2 than on Fig. 1. Fig. 1 shows the cathode of diode "29" connecting to contact "22"; whereas, Fig. 2 shows the cathode of diode "29" connecting to contact "26."

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application.

Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

The disclosure is objected to because of the following informalities: The specification uses different wording to describe the same component(s) as shown in the figures. The specification describes character references that do not exist in the described figure(s). Below are some examples.

The character "86" is used to describe a poly gate (page 8 line 28-29), a control gate (page 9 line 6), a tang (page 6 line 36), and both a control gate and a tang in the same line (page 9 line 12-13).

The following reference sign(s) are mentioned in the description but not shown in the respective figures: "31" (Page 6 line 30, see Fig. 2), "90" (Page 7 line 23, see Fig. 2). Examiner assumes that applicant intended "31" to be "21."

Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. **Claims 21 are rejected under 35 U.S.C. 102(b) as being anticipated by Wong U.S. Patent No. 6,345,000.**

Regarding independent claim 21, Wong '000 shows a memory array that is capable of performing write operations simultaneously to erase operations within the same array (page 2, line 53-55).

Allowable Subject Matter

Claim 1-12 and 20 allowed.

With respect to claim 1, the following is an examiner's statement of reasons for allowance: There is no teaching or suggestion in prior art to a poly plate, connected to a memory transistor and current injector, that is capacitively coupled to a word line.

With respect to claim 20, the following is an examiner's statement of reasons for allowance: There is no teaching or suggestion in prior art to a poly plate, connected to a memory transistor and current injector, that is capacitively coupled to a word line.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure: Wong US Pub. No. 2002/0149986A1, Grise et al. US Pat. No. 4,375,085, Yamashita et al. US Pat. 6,026,022, Wong et al. US Pat. 5,949,716, and Cook et al. US Pat. 4,434,478.

Wong '986 shows a grouping of memory arrays with plural word lines, row lines, column lines, and control lines. The circuit performs write and erase operations simultaneously; however, only one operation can be performed on a distinct array. Thus, an erase operation on one array can be simultaneous to a write operation on a different array.

Grise et al. '085 shows a memory array with plural word lines (Fig. 2 [WL1, WL2]), plural bit lines (Fig. 2 [BL1, BL2]), and plural program lines (Fig. 2 [T11, T12]). There is a multiplicity of memory cells between word lines. A word line is connected to a control gate (page 3, line 14). The control gate is a component of

the channel region that is capacitively coupled to a floating plate (page 3, line 16-18). A current injector is formed over a floating plate (page 3, line 54-55). Two different locations in the array can be written simultaneously when applied with the same voltage (page 6, line 61-64). It is well-known in the art that writing "0's" is synonymous with erasing; hence, writing and erasing in this context are applicably synonymous. However, this particular patent does not show a poly plate, coupled to the current injector and the memory transistor, receiving a capacitively induced voltage from a word line

Yamashita et al. '022 shows a memory device with plural word lines, plural bit lines, plural page lines, plural address lines, and plural digit lines (page 1, line 38-41). Each memory cell is made of a memory cell transistor and an n-channel MOS transistor (page 3, line 1-2). The circuit can simultaneously write to different addresses; however, the n-channel MOS transistor does not function as a current injector. Furthermore, the structure of the memory cell is not shown, with respect to transistors connecting to a poly plate capacitively coupled to a word line

Wong et al. '716 shows a memory with two memory arrays connected. This patent provides clarity with respect to the definition of "sector," as meaning a grouping of columns of memory cells (page 3, line 24-25). The arrays have plural column lines (Fig.1 [CL0, CL1]), plural row lines (Fig. 1 [LRL0, LRL1, RRL0, RRL1]) and plural source lines (Fig. 1 [LSL0, LSL1, RSL0, RSL1[). The circuit can erase from one memory array while simultaneously writing to the other array(page 5, line 51-53) . However, this circuit does not show the structure of

the memory cell, with respect to transistors connecting to a poly plate capacitively coupled to a word line. Also, an electron/current injector is not shown.

Cook et al. '478 shows a memory system with plural word lines (Fig. 1 [WL1, WL2]), plural bit lines (Fig. 1 [BL1, BL2]), and plural control lines (Fig. 1 [CL1, CL2]). There is a multiplicity of memory cells (Fig. 1 [10A, 10B]) between the word lines. Each memory cell has two transistors (Fig. 1 [T1, T2]). However, structure of the memory cell is not shown, with respect to transistors connecting to a poly plate capacitively coupled to a word line. Also, this device does not perform simultaneous write and erase.

When responding to this office action, applicants are advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist the examiner in locating appropriate paragraphs.

A shortened statutory period for response to this action is set to expire three months and zero days from the date of this letter. Failure to respond within the period for response will cause this application to become abandoned (see MPEP 710.02(b)).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander Sofocleous whose telephone number is 571-272-0635. The examiner can normally be reached on 7:00am - 4pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on 571-272-1869. The fax

phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AGS

ANH PHUNG
PRIMARY EXAMINER